EDU SCHOOL
ijpsrs.com

INTERNATIONAL JOURNAL OF PURE SCIENCE RESEARCH STUDIES (IJPSRS)
(Open Access, Double-Blind Peer Reviewed Journal)
ISSN Online: ISSN Print

Quantum Tunneling in Semiconductors: Computing Implications

Vimala George

Associate Professor, Department of Physics, St. Xavier's College for Women (Autonomous), Aluva, India.

Article Information
Received: 6th November 2025
Received in revised form: 8th December 2025
Accepted: 9th January 2025
Available online:14th February 2026
Volume: 2
Issue: 1
DOI: https://doi.org/10.5281/zenodo.18668391

Abstract

Quantum tunneling represents a fundamental quantum mechanical phenomenon wherein particles penetrate energy barriers that would be classically insurmountable. In semiconductor physics, this effect has evolved from a theoretical curiosity to a critical operational mechanism with profound implications for modern computing technologies. This paper examines the theoretical foundations of quantum tunneling in semiconductor materials, analyzes its manifestations in contemporary electronic devices, and evaluates its significance for next-generation computing architectures. Through examination of tunnel field-effect transistors (TFETs), resonant tunneling diodes (RTDs), and emerging quantum computing platforms, we demonstrate that quantum tunneling simultaneously presents engineering challenges in nanoscale device fabrication and unprecedented opportunities for computational advancement. Our analysis reveals that as semiconductor device dimensions approach atomic scales, tunneling effects transition from parasitic phenomena to essential operational principles, fundamentally reshaping transistor design paradigms and enabling novel computational architectures with potential performance improvements exceeding several orders of magnitude over conventional technologies.

Keywords: Quantum Tunneling, Semiconductor Devices, Tunnel Field-Effect Transistors, Resonant Tunneling Diodes,Quantum Computing, Band-To-Band Tunneling.

1. INTRODUCTION

The relentless miniaturization of semiconductor devices, driven by Moore's Law for over five decades, has propelled transistor dimensions into the nanoscale regime where quantum mechanical effects dominate device behavior.[1] Among these quantum phenomena, tunnelling the probability-based penetration of potential barriers by particles has emerged as both a formidable challenge to conventional device scaling and a promising mechanism for revolutionary computing paradigms. Classical semiconductor physics, grounded in drift-diffusion models and thermionic emission, becomes increasingly inadequate as gate lengths shrink below 10 nanometers, necessitating quantum transport frameworks to accurately predict and engineer device characteristics.[2]

Quantum tunneling manifests in semiconductors through several distinct mechanisms, each with unique implications for device operation. Direct band-to-band tunneling (BTBT) in heavily doped p-n junctions, Fowler-Nordheim tunneling through thin oxides, and trap-assisted tunneling via defect states collectively determine leakage currents in nanoscale transistors, fundamentally limiting the continued scaling of complementary metal-oxide-semiconductor (CMOS) technology.[3] Simultaneously, controlled exploitation of tunneling phenomena has enabled novel device concepts including tunnel field-effect transistors with sub-60 mV/decade subthreshold slopes, resonant tunneling diodes exhibiting negative differential resistance, and quantum dots leveraging discrete energy states for quantum information processing.[4,5]

This paper provides a comprehensive examination of quantum tunneling in semiconductor devices, structured as follows: Section 2 reviews the theoretical foundations and mathematical formalism governing tunneling processes; Section 3 analyzes specific manifestations in contemporary semiconductor devices; Section 4 discusses implications for next-generation computing architectures including quantum and neuromorphic systems; and Section 5 synthesizes these findings to project future research directions and technological trajectories.

2. THEORETICAL FOUNDATIONS OF QUANTUM TUNNELING

2.1. Quantum Mechanical Formalism

Quantum tunneling emerges as a direct consequence of the wave nature of matter, described mathematically by the Schrödinger equation. For a one-dimensional potential barrier of height V_0 and width a, the time-independent Schrödinger equation governs particle behavior:

$$-\frac{\hbar^2}{2m}\frac{d^2\psi}{d\varkappa^2} + V(x)\,\psi\,(x) = E\psi(\varkappa)$$

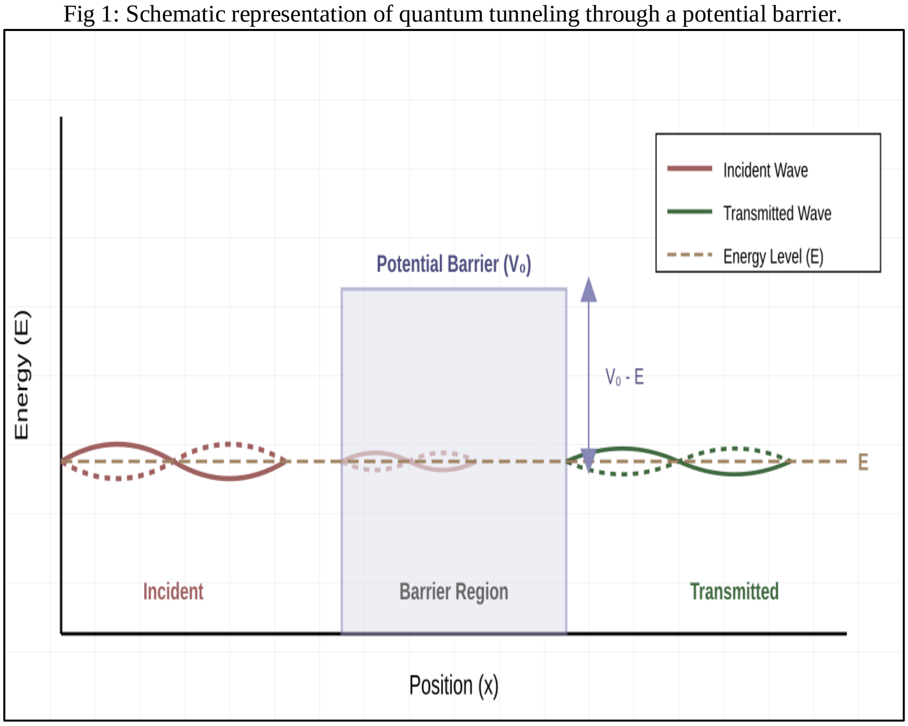
where ψ represents the wavefunction, E the particle energy, m the effective mass, and $\hbar$ the reduced Planck constant.[6] Unlike classical particles that exhibit deterministic reflection when $E < V_0$, quantum particles possess finite probability amplitudes extending beyond the barrier boundaries.

For a rectangular barrier, the transmission probability T, representing the likelihood of successful barrier penetration, is approximated by the WKB (Wentzel-Kramers-Brillouin) method as $T \approx e^{-2Ka}$, where

$$K = \frac{\sqrt{(2m(V_0 - E)}}{\hbar}$$

Defines the decay constant within the barrier region.[7] This exponential dependence on barrier width and height fundamentally distinguishes quantum from classical behavior, as illustrated in Figure 1.

Fig 1: Schematic representation of quantum tunneling through a potential barrier.

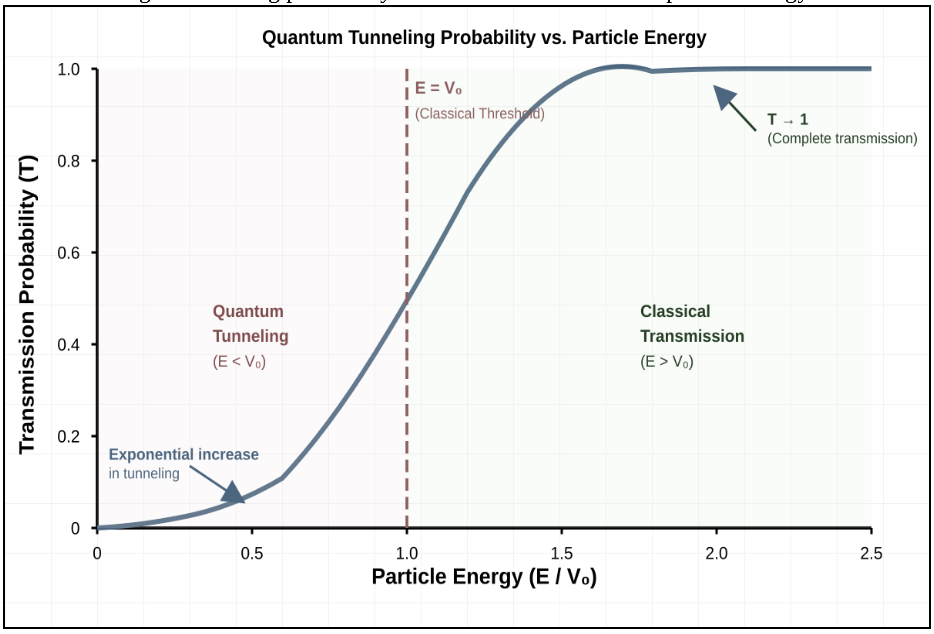


The incident wave (red) partially transmits through the classically forbidden region (blue shaded), resulting in a transmitted wave (green) with reduced amplitude. Energy level E remains constant throughout, while the wavefunction exhibits exponential decay within the barrier.

2.2. Energy Dependence and Transmission Characteristics

The transmission probability exhibits strong energy dependence, increasing exponentially as particle energy approaches the barrier height. Figure 2 illustrates this relationship, demonstrating the transition from pure quantum tunneling ($E << V_0$) to classical over-barrier transmission ($E > V_0$). This behavior fundamentally governs current-voltage characteristics in tunnel devices, where small voltage changes induce dramatic current variations through exponential modulation of barrier transparency.

Fig 2: Tunneling probability as a function of normalized particle energy.



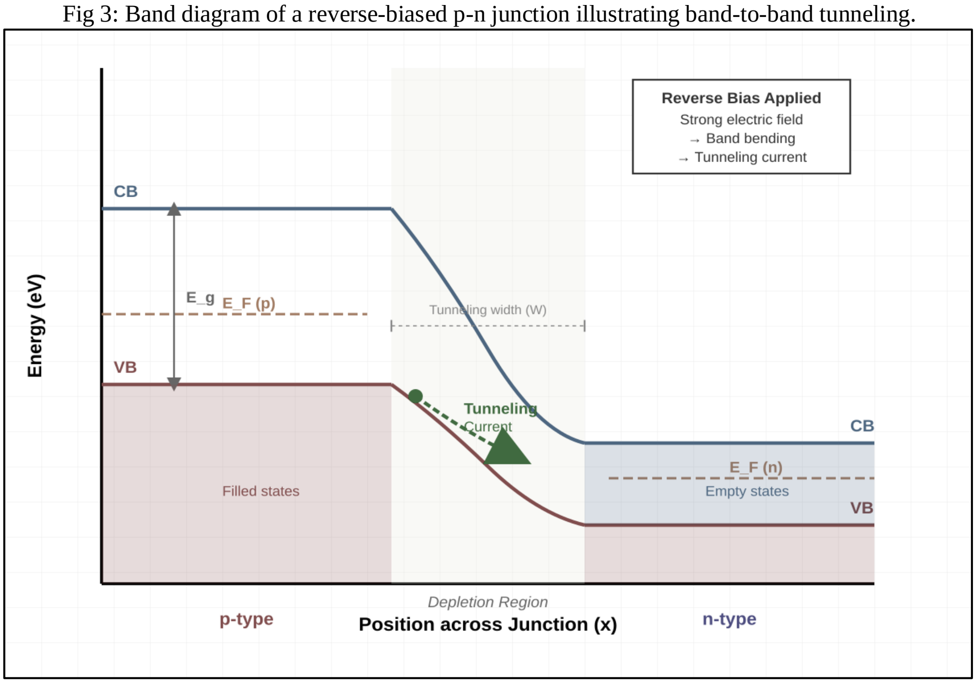
The shaded regions demarcate quantum tunneling ($E < V_0$, red) from classical transmission ($E > V_0$, green) regimes. Note the exponential increase in transmission probability approaching the classical threshold, with $T \rightarrow 1$ for $E >> V_0$.

3. TUNNELING PHENOMENA IN SEMICONDUCTOR DEVICES

3.1. Band-to-Band Tunneling in p-n Junctions

In heavily doped p-n junctions under reverse bias, band-to-band tunneling constitutes a dominant current mechanism when electric fields exceed approximately 1 MV/cm.[8] As depicted in Figure 3, strong band bending creates spatial alignment between filled valence band states on the p-side and empty conduction band states on the n-side, enabling direct electron tunneling across the forbidden gap. The tunneling current density follows the form $J \propto E^2 \exp(-B/E)$, where E represents the electric field and B is a material-dependent constant incorporating the bandgap energy and effective masses (Kane, 1961).[9]

Fig 3: Band diagram of a reverse-biased p-n junction illustrating band-to-band tunneling.



Strong electric fields in the depletion region (yellow shaded) induce severe band bending, aligning the valence band on the p-side with the conduction band on the n-side. Electrons tunnel directly from filled valence states to empty conduction states (green arrow), generating tunneling current. CB: conduction band; VB: valence band; E_F: Fermi level.

3.2. Tunnel Field-Effect Transistors

Tunnel field-effect transistors exploit band-to-band tunneling as their primary switching mechanism, offering theoretical subthreshold slopes below the 60 mV/decade limit of conventional MOSFETs at room temperature.[4] This thermal limit arises from the Boltzmann distribution of carrier energies in thermionic emission, while tunneling-based switching depends on barrier transparency modulation rather than thermal activation. TFETs employ a p-i-n structure where gate voltage controls the tunneling barrier width at the source-channel interface, enabling steep switching characteristics with potentially dramatic reductions in off-state leakage and operating voltage.[5]

Despite promising theoretical predictions, practical TFET implementations face significant challenges including low on-state currents, sensitivity to interface trap states, and difficulties achieving sub-60 mV/decade operation across multiple current decades.[10] Advanced approaches incorporating heterojunctions, strained silicon-germanium alloys, and III-V compound semiconductors with smaller effective masses and direct bandgaps have demonstrated improved performance, though fabrication complexity and reliability concerns persist.

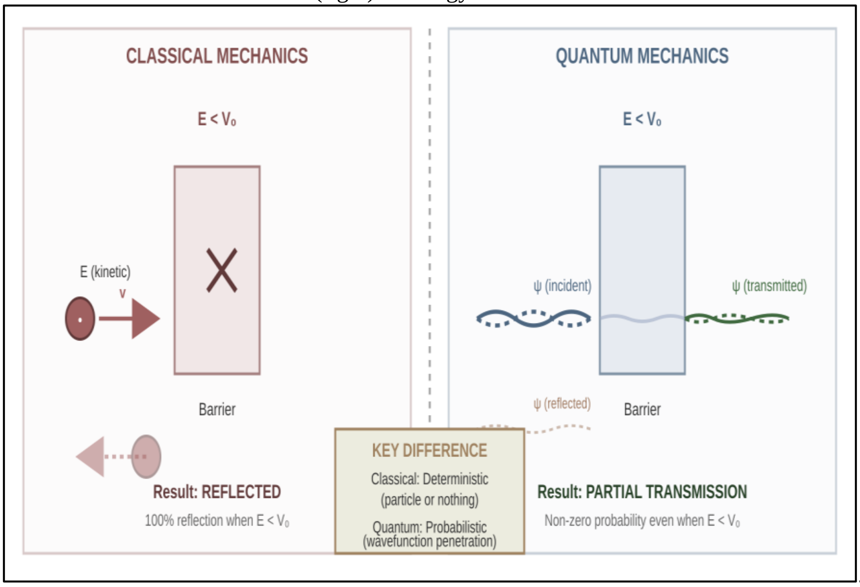
3.3. Gate Oxide Tunneling and Leakage Mechanisms

As CMOS technology scaled gate oxide thickness below 2 nm, direct quantum mechanical tunneling through the insulator emerged as a primary leakage path, fundamentally limiting further thickness reduction.[3] Fowler-Nordheim tunneling dominates at high electric fields when carriers tunnel through triangular barriers, while direct tunneling becomes significant in ultra-thin oxides where the barrier approximates a rectangular profile. The transition from SiO_2 to high-κ dielectrics such as HfO_2 partially mitigated tunneling leakage by enabling physically thicker layers with equivalent electrical capacitance, though trap-assisted tunneling through defect states remains a concern.[11]

3.4. Quantum versus Classical Transport Regimes

The fundamental distinction between classical and quantum particle transport becomes crucial in nanoscale semiconductor devices. Figure 4 contrasts these regimes, illustrating how quantum mechanics permits barrier penetration forbidden by classical physics. This dichotomy underlies the paradigm shift in semiconductor device physics, where design methodologies must transition from purely classical drift-diffusion models to quantum transport frameworks incorporating wavefunction coherence, tunneling probabilities, and quantum interference effects.

Fig 4: Comparative illustration of classical mechanics (left) versus quantum mechanics (right) at energy barriers



Classical particles experience deterministic reflection when kinetic energy falls below barrier height, while quantum particles exhibit probabilistic behavior with non-zero transmission probability. The wavefunction (ψ) penetrates the classically forbidden barrier region, enabling partial transmission even when $E < V_0$.

4. IMPLICATIONS FOR NEXT-GENERATION COMPUTING

4.1. Quantum Computing Architectures

Quantum tunneling constitutes a foundational mechanism for semiconductor-based quantum computing implementations, particularly in silicon spin qubit architectures.[12] Tunnel coupling between adjacent quantum dots enables controlled two-qubit gate operations through exchange interactions, where tunneling rates directly determine gate fidelities and operational speeds. Precise engineering of tunnel barriers via electrostatic gates permits dynamic modulation of inter-dot coupling, essential for implementing universal quantum gate sets while maintaining sufficient qubit isolation to preserve quantum coherence.[13]

Furthermore, resonant tunneling through discrete energy levels in quantum dots enables single-electron control and charge sensing mechanisms critical for qubit readout. The exquisite sensitivity of tunneling currents to electrostatic potential variations permits charge detection with resolution approaching individual elementary charges, facilitating rapid, high-fidelity quantum state measurement.[14] As quantum computing transitions from laboratory demonstrations toward practical quantum advantage, semiconductor tunneling phenomena will remain central to device physics and architectural design.

4.2. Ultra-Low-Power Computing

The sub-thermal subthreshold slope of ideal TFETs presents transformative opportunities for ultra-low-power computing applications where static power dissipation dominates energy budgets. Conventional CMOS transistors face a fundamental 60 mV/decade limit at 300 K due to thermal broadening of the Fermi-Dirac distribution, constraining minimum operating voltages to approximately 0.5-0.7 V to maintain acceptable on/off current ratios.[15] TFETs, exploiting the sharp energy filtering inherent in quantum tunneling, theoretically achieve sub-10 mV/decade switching, potentially enabling operation at supply voltages below 0.2 V with orders-of-magnitude reductions in standby power consumption.

Such dramatic power reductions would profoundly impact mobile computing, Internet-of-Things sensor networks, and biomedical implantable devices where battery lifetime and thermal constraints dictate system capabilities. However, realizing these benefits requires overcoming persistent challenges in achieving high on-currents, minimizing parasitic capacitances, and developing manufacturable, reliable fabrication processes compatible with existing CMOS infrastructure.[10]

4.3. Neuromorphic and Non-von Neumann Architectures

Resonant tunneling diodes exhibiting negative differential resistance enable novel neuromorphic computing paradigms and non-Boolean logic operations.[16] The intrinsic current-voltage nonlinearity of RTDs provides compact, energy-efficient implementations of threshold activation functions central to artificial neural networks. Furthermore, the picosecond-scale tunneling timescales support ultra-high-speed oscillators and multi-valued logic circuits operating in the terahertz frequency regime, substantially exceeding conventional CMOS switching speeds.

Hybrid architectures combining resonant tunneling devices with conventional CMOS have demonstrated feasibility for spike-timing-dependent plasticity circuits, cellular neural networks, and other brain-inspired computing models.[17] As machine learning workloads increasingly dominate computing demands, specialized accelerators leveraging quantum tunneling phenomena may offer decisive advantages in computational efficiency and throughput compared to general-purpose von Neumann architectures.

5. CONCLUSION

Quantum tunneling in semiconductors exemplifies the dual nature of quantum mechanical effects in nanoscale electronics: simultaneously constraining conventional technology scaling while enabling transformative device concepts and computational paradigms. As transistor dimensions inexorably approach atomic scales, tunneling transitions from a parasitic leakage mechanism requiring mitigation to a fundamental operational principle demanding precise control and exploitation. This paper has examined the theoretical foundations of quantum tunneling, analyzed its manifestations in contemporary semiconductor devices including TFETs and resonant tunneling structures, and evaluated implications for emerging computing architectures.

The path forward requires sustained research addressing persistent challenges in materials science, device physics, and circuit design. Achieving sub-60 mV/decade switching with adequate on-currents demands innovative heterostructures, optimized doping profiles, and possibly topological materials with unconventional band structures. Integration of tunneling-based devices into manufacturable, reliable processes compatible with existing semiconductor infrastructure presents substantial engineering challenges requiring close collaboration between academia and industry. Successfully navigating these challenges promises revolutionary advances in quantum computing, ultra-low-power electronics, and neuromorphic systems computing paradigms fundamentally enabled by quantum tunneling phenomena that seemed merely curious academic exercises mere decades ago.

Future research directions include exploration of two-dimensional materials such as graphene and transition metal dichalcogenides exhibiting ultrashort tunneling lengths, investigation of topological insulators with protected edge states for coherent tunneling transport, and development of hybrid quantum-classical systems leveraging tunneling for quantum state preparation and measurement. As semiconductor technology continues evolving toward the ultimate limits imposed by atomic discreteness and quantum uncertainty, quantum tunneling will undoubtedly remain central to both fundamental physics understanding and practical technological innovation.

REFERENCES

1. Colinge J-P, Greer JC. 2016. *Nanowire transistors: physics of devices and materials in one dimension*. Cambridge: Cambridge University Press. https://doi.org/10.1017/CBO9781107280779
2. Lundstrom M, Jeong C. 2013. *Near-equilibrium transport: fundamentals and applications*. Singapore: World Scientific Publishing. https://doi.org/10.1142/7975
3. Taur Y, Ning TH. 2021. *Fundamentals of modern VLSI devices*. 3rd ed. Cambridge: Cambridge University Press. https://doi.org/10.1017/9781108847087
4. Ionescu AM, Riel H. 2011. Tunnel field-effect transistors as energy-efficient electronic switches. *Nature*. 479(7373):329–337. https://doi.org/10.1038/nature10679
5. Seabaugh AC, Zhang Q. 2010. Low-voltage tunnel transistors for beyond CMOS logic. *Proc IEEE*. 98(12):2095–2110. https://doi.org/10.1109/JPROC.2010.2070470
6. Griffiths DJ. 2018. *Introduction to quantum mechanics*. 3rd ed. Cambridge: Cambridge University Press.
7. Razavy M. 2003. *Quantum theory of tunneling*. Singapore: World Scientific Publishing. https://doi.org/10.1142/4984
8. Sze SM, Ng KK. 2006. *Physics of semiconductor devices*. 3rd ed. Hoboken (NJ): John Wiley & Sons.
9. Kane EO. 1961. Theory of tunneling. *J Appl Phys*. 32(1):83–91. https://doi.org/10.1063/1.1735965
10. Lu H, Seabaugh A. 2014. Tunnel field-effect transistors: state-of-the-art. *J Electron Devices Soc*. 2(4):44–49. https://doi.org/10.1109/JEDS.2014.2326622
11. Robertson J. 2006. High dielectric constant gate oxides for metal oxide Si transistors. *Rep Prog Phys*. 69(2):327–396. https://doi.org/10.1088/0034-4885/69/2/R02
12. Veldhorst M, Yang CH, Hwang JCC, Huang W, Dehollain JP, Muhonen JT, et al. 2015. A two-qubit logic gate in silicon. *Nature*. 526(7573):410–414. https://doi.org/10.1038/nature15263
13. Loss D, DiVincenzo DP. 1998. Quantum computation with quantum dots. *Phys Rev A*. 57(1):120–126. https://doi.org/10.1103/PhysRevA.57.120
14. Barthel C, Reilly DJ, Marcus CM, Hanson MP, Gossard AC. 2009. Rapid single-shot measurement of a singlet-triplet qubit. *Phys Rev Lett*. 103(16):160503. https://doi.org/10.1103/PhysRevLett.103.160503
15. Nikonov DE, Young IA. 2013. Overview of beyond-CMOS devices and a uniform methodology for their benchmarking. *Proc IEEE*. 101(12):2498–2533. https://doi.org/10.1109/JPROC.2013.2252317
16. Datta S, Salahuddin S, Behin-Aein B. 2012. Non-volatile spin switch for Boolean and non-Boolean logic. *Appl Phys Lett*. 101(25):252411. https://doi.org/10.1063/1.4769989
17. Merolla PA, Arthur JV, Alvarez-Icaza R, Cassidy AS, Sawada J, Akopyan F, et al. 2014. A million spiking-neuron integrated circuit with a scalable communication network and interface. *Science*. 345(6197):668–673. https://doi.org/10.1126/science.1254642